WHAT IS CLAIMED IS:

1. A subarray control circuit, comprising:

a wordline driver configured to generate a wordline activation signal;

a write/read control signal generator configured to generate a write/read enable signal; and

a timing generator configured to generate a wordline timing signal input to the wordline driver and a write/read timing signal input to the write/read control signal generator, the wordline activation signal based on the wordline timing signal and the write/read enable signal based on the write/read timing signal.

2. The subarray control circuit as recited in Claim 1, wherein the wordline driver comprises a latch coupled to a logic circuit.

3. The subarray control circuit as recited in Claim 2, wherein the logic circuit is configured to receive the wordline timing signal and generate the wordline activation signal based on the wordline timing signal.

4. The subarray control circuit as recited in Claim 1, wherein the write/read control signal generator is a sense amplifier enable generator comprising a latch coupled to a logic circuit, the write/read enable signal is a sense amplifier enable signal, and the write/read timing signal is a sense amplifier timing signal.

5. The subarray control circuit as recited in Claim 4, wherein the logic circuit is configured to receive the sense amplifier timing signal and generate the sense amplifier enable signal based on the sense amplifier timing signal.

6. The subarray control circuit as recited in Claim 1, further comprising a global clock distribution circuit configured to distribute a global clock signal to the timing generator.

7. The subarray control circuit as recited in Claim 6, wherein the wordline timing signal and write/read timing signal are based on the global clock signal.

8. A method of accessing subarray cells in a memory module, comprising:

generating a wordline activation signal using a wordline driver;

generating a write/read enable signal using a write/read control signal generator; and

generating a wordline timing signal and a write/read timing signal using a timing generator, and inputting the wordline timing signal into the wordline driver and the write/read timing signal into the write/read control signal generator, the wordline activation signal based on the wordline timing signal and the write/read enable signal based on the write/read timing signal.

9. The method as recited in Claim 8, wherein generating a wordline activation signal comprises generating a wordline activation signal using a wordline driver having a latch coupled to a logic circuit.

10. The method as recited in Claim 9, wherein generating a wordline activation signal further comprises capturing wordline enable data using a latching circuit and launching the wordline activation signal through a logic circuit based on the wordline timing signal.

11. The method as recited in Claim 8, wherein generating a write/read enable signal comprises generating a sense amplifier enable signal using a sense amplifier enable generator having a latch coupled to a logic circuit.

12. The method as recited in Claim 8, wherein generating a write/read enable signal comprises capturing circuit enable data using a latching circuit and launching the write/read enable signal through a logic circuit based on the write/read timing signal.

13. The method as recited in Claim 8, further comprising distributing a global clock signal to the timing generator using a global clock distribution circuit.

14. The method as recited in Claim 13, wherein generating a wordline timing signal and a write/read timing signal comprises generating a wordline timing signal and a write/read timing signal based on the global clock signal.

15. A memory module, comprising:

a subarray of cells configured to be activated or deactivated using a wordline activation signal; and

a subarray control circuit coupled to the subarray of cells, comprising:

a wordline driver configured to generate the wordline activation signal;

a write/read control signal generator configured to generate a write/read enable signal; and

a timing generator configured to generate a wordline timing signal input to the wordline driver and a write/read timing signal input to the write/read control signal generator, the wordline activation signal based on the wordline timing signal and the write/read enable signal based on the write/read timing signal.

16. The memory module as recited in Claim 15, wherein the wordline driver comprises a latch coupled to a logic circuit.

17. The memory module as recited in Claim 16, wherein the logic circuit is configured to receive the wordline timing signal and generate the wordline activation signal based on the wordline timing signal.

18. The memory module as recited in Claim 15, wherein the write/read control signal generator is a sense amplifier enable generator comprising a latch coupled to a logic circuit, the write/read enable signal is a sense amplifier enable signal, and the write/read timing signal is a sense amplifier timing signal.

19. The memory module as recited in Claim 18, wherein the logic circuit is configured to receive the sense amplifier timing signal and generate the sense amplifier enable signal based on the sense amplifier timing signal.

20. The memory module as recited in Claim 15, further comprising a global clock distribution circuit configured to distribute a global clock signal to the timing generator, the wordline timing signal and write/read timing signal based on the global clock signal.